1.6G Bicmos 工艺 PLL IP

The PLL consists of a buffer amplifier, multi-modlus prescaler (divide by 4,5,6 and 7), a 6-bit programmable post divider, and charge pump. The loop divider consists of three 25-bit accumulators. The PLL may use reference frequencies of 13 to 26MHz. the loop divider is programmed via the ND and the NUM SPI words. The ND <7:0> represents the prescaler (2-bit)

And the loop divider (6-bit) control word. The PLL's pattern generator also accepts the NUM <24:0> word that is the numerator of the fractional divisor.

VCO gain: 304.91 MHz/V

VCO output: 488.00mV

Phase noise: -105.45 @100k

Tuning range: 397.68 MHz (Vtune=0.5V～2.3V)

Target frequency: 1.57G @vtune = 1.4V