USB 2.0 IP core

Feature

- Full compliance with the USB 2.0 specification
- Up to 15 configurable for 15 IN and 15 OUT endpoints
  Programmable Endpoints size
  Configurable endpoints buffer
  Programmable endpoint type
- Fixed control endpoint 0
- Configurable 32, 16, or 8-bit microprocessor interface
- Rich interrupt vector
- Flexible interrupt request
- Ready for external DMA module
- Suspend and resume power management functions
- Remote Wake-Up function
- UTMI Transceiver Macro cell Interface

Introduction

The Microlinks USB20 *High Speed Device Controller* core provides a USB function controller that has been certified compliant with the USB 2.0 specification for high/full-speed (480/12 Mbps) functions. The core is user-configurable for up to 15 IN endpoints and/or up to 15 OUT endpoints in addition to Endpoint 0, and includes power management and remote wake-up functions..

Each endpoint requires a FIFO to be associated with it. The Core has a RAM interface for connecting to a single block of synchronous two-port RAM, which is used for all the endpoint FIFOs. (The RAM block itself needs to be added by the user.)

The size of the FIFO for Endpoint 0 is fixed at 64 bytes and can buffer 1 packet. Core's FIFO interface is configurable with regard to the other endpoint FIFOs that may be from 4 to 4096 bytes in size.

The Core provides a USB 2.0 Transceiver Macrocell Interface (UTMI Specification version 1.05) to connect to an 8/16-bit high/full-speed transceiver. The design is also offered with a choice of high-level 32bit, 16bit, 8-bit microcontroller interfaces. In the base model, access to the FIFOs and the internal control/status registers is via a 8/16/32-bit interface to connect to a processor bus. The Core provides all the USB packet encoding, decoding, checking and handshaking – interrupting the CPU only when endpoint data has been successfully transferred. After a power-up reset, the Core is placed in 'Powered' state with the registers set.

Designed for easy reuse, a typical minimum configuration of the core requires <10k ASIC gates.